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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/074,265	02/12/2002	Nicholas Pavey	S01022/80847	5021
23628	7590	09/23/2005	EXAMINER	
WOLF GREENFIELD & SACKS, PC FEDERAL RESERVE PLAZA 600 ATLANTIC AVENUE BOSTON, MA 02210-2211			JONES, HUGH M	
			ART UNIT	PAPER NUMBER
			2128	
DATE MAILED: 09/23/2005				

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/074,265	PAVEY, NICHOLAS	
	Examiner	Art Unit	
	Hugh Jones	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE _____ MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 12 February 2002.
 2a) This action is **FINAL**. 2b) This action is non-final.
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-6 is/are pending in the application.
 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
 5) Claim(s) _____ is/are allowed.
 6) Claim(s) 1-6 is/are rejected.
 7) Claim(s) _____ is/are objected to.
 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.
 10) The drawing(s) filed on 22 May 2002 is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) Notice of References Cited (PTO-892)
 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
 3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
 Paper No(s)/Mail Date _____

4) Interview Summary (PTO-413)
 Paper No(s)/Mail Date. _____

5) Notice of Informal Patent Application (PTO-152)
 6) Other: _____

DETAILED ACTION

1. Claims 1-6 of U. S. Application 10/074,265, filed 02/12/2002, are presented for examination.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-6 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Hollander et al..

4. Hollander et al. disclose :

A method of verifying a digital hardware design simulated in hardware design language (col. 5, lines 44-52), including the steps of:

defining at least one state to be verified, the state including a signal value for each a plurality of components within the hardware design (fig. 1, col. 3; col. 4, line 39 to col. 5, 4line 4; col. 5, line 63 to col. 6, line 22);

applying a test to the hardware design (fig. 1, col. 3; col. 4, line 39 to col. 5, 4line 4; col. 5, line 63 to col. 6, line 22);

generating traces of internal signals within the hardware design during the test, each trace including signal data and time data and including least the internal signals associated with the components (fig. 1, col. 3; col. 4, line 39 to col. 5, 4line 4; col. 5, line 63 to col. 6, line 22);

processing the traces to ascertain whether the plurality of components simultaneously had the signal values associated with the state, thereby ascertain whether the state was achieved (fig. 1, col. 3; col. 4, line 39 to col. 5, 4line 4; col. 5, line 63 to col. 6, line 22).

wherein more than one state defined, each state having signal value for each of a plurality components of the hardware design (fig. 1, col. 3; col. 4, line 39 to col. 5, 4line 4; col. 5, line 63 to col. 6, line 22),

the traces being processed to ascertain, for each state, whether the corresponding plurality of components simultaneously had the signal values associated with the state; thereby ascertain whether each of the states was achieved (fig. 1, col. 3; col. 4, line 39 to col. 5, 4line 4; col. 5, line 63 to col. 6, line 22).

wherein the processing step includes ascertaining whether predetermined sequence of states was achieved (fig. 1, col. 3; col. 4, line 39 to col. 5, 4line 4; col. 5, line 63 to col. 6, line 22).

wherein the processing step includes ascertaining whether given state in a sequence was achieved within predetermined time period after an earlier state in the sequence (fig. 1, col. 3; col. 4, line 39 to col. 5, 4line 4; col. 5, line 63 to col. 6, line 22).

wherein the traces are pre-processed prior to the processing step, such that, for at least each of the components defined within each of the states, a value for the respective signals associated with those components exists for each time for which the traces are to be processed (fig. 1, col. 3; col. 4, line 39 to col. 5, 4line 4; col. 5, line 63 to col. 6, line 22).

wherein one or more of the signal values are values of a field associated with the corresponding component (fig. 1, col. 3; col. 4, line 39 to col. 5, 4line 4; col. 5, line 63 to col. 6, line 22).

5. Any inquiry concerning this communication or earlier communications from the examiner should be:

directed to: Dr. Hugh Jones telephone number (571) 272-3781,

Monday-Thursday 0830 to 0700 ET,

or

the examiner's supervisor, Jean Homere, telephone number (571) 272-3780.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist, telephone number (703) 305-3900.

mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 308-9051 (for formal communications intended for entry)

or (703) 308-1396 (for informal or draft communications, please label *PROPOSED* or *DRAFT*).

Dr. Hugh Jones

Primary Patent Examiner

August 3, 2005

HUGH JONES Ph.D.
PRIMARY PATENT EXAMINER
TECHNOLOGY CENTER 2102